REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-69 are presently active.

In the outstanding Office Action, Claims 1-69 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claims 1-44, 1-58, 1-48, 1-78, and 1-62 of co-pending Application Nos. 10/673,138; 10/673,467; 10/673,501; 10/673,507; 10/673,583; and 10/673,583, respectively. Claims 1-25, 32-56 and 63-69 were rejected under 35 U.S.C. § 103(a) as being obvious over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Kee et al (U.S. Pat. No. 5,583,780). Claims 26-31 and 57-59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al and Kee et al in view of Fatke et al (U.S. Pat. Appl. No. 200510016947).

Regarding the rejection on the merits:

Claim 1 defines a method for analyzing a process performed by a semiconductor processing tool including:

> 1) inputting process data relating to an actual process being performed by the semiconductor processing tool,
> 2) inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool,
> 3) performing a first principles simulation for the actual process being performed ***during performance of the actual process*** using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and
> 4) using the first principles simulation result ***obtained during the performance of the actual process*** to determine a fault in the actual process being performed by the semiconductor processing tool.[1]

[1] The enumerations have been added purely for the purpose of referencing these elements for discussion.

The Office Action states on page 14 that it is common knowledge to practitioners in the art to recognize that performing the simulation environment (a first principles simulation) is performing the simulation environment for the actual process being performed. Yet, the art of record does not show this to be true. Rather, the art of record shows that the simulations are performed before a process is run. This is because the simulation process as described in Kee et al is "a lengthy and costly intensive process" and therefore would not be compatible with real-time process control in which, as defined in the claims, a first principles simulation is performed for the actual process being performed ***during performance of the actual process***.

The examiner reads as relevant to this claimed feature Sonderman et al (at least col. 7, line 7, to col. 9, line 51). From this disclosure, Applicant respectfully points out that, at col. 9, lines 46-51 Sonderman et al. specifically discloses:

> The system 100 then optimizes the simulation (described above) ***to find more optimal process target*** (T_i) for each silicon wafer, S_i ***to be processed***. These target values are then used ***to generate new control inputs***, X_{Ti}, on the line 805 to control ***a subsequent process*** of a silicon wafer S_i. The ***new control inputs***, X_{Ti}, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like. [Emphasis added]

Thus, this section of Sonderman et al clearly discloses that the simulation is to find a more optimum process target for each silicon wafer ***to be processed***. The simulation results produce a new control input for the silicon wafer ***to be processed***. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process to be performed ***before*** performance of the actual process, and **not** the claimed performing first principles simulation ***for the actual process being performed during performance of the actual process***.

Other sections of Sonderman et al. support Applicant's position on this matter.

For instance, reproduced below is Figure 4 of Sonderman et al which clearly shows that the simulation results are produced ***ahead of performing a process*** and thus have to be based on historical data, and not based on the actual process being performed during performance of the actual process.

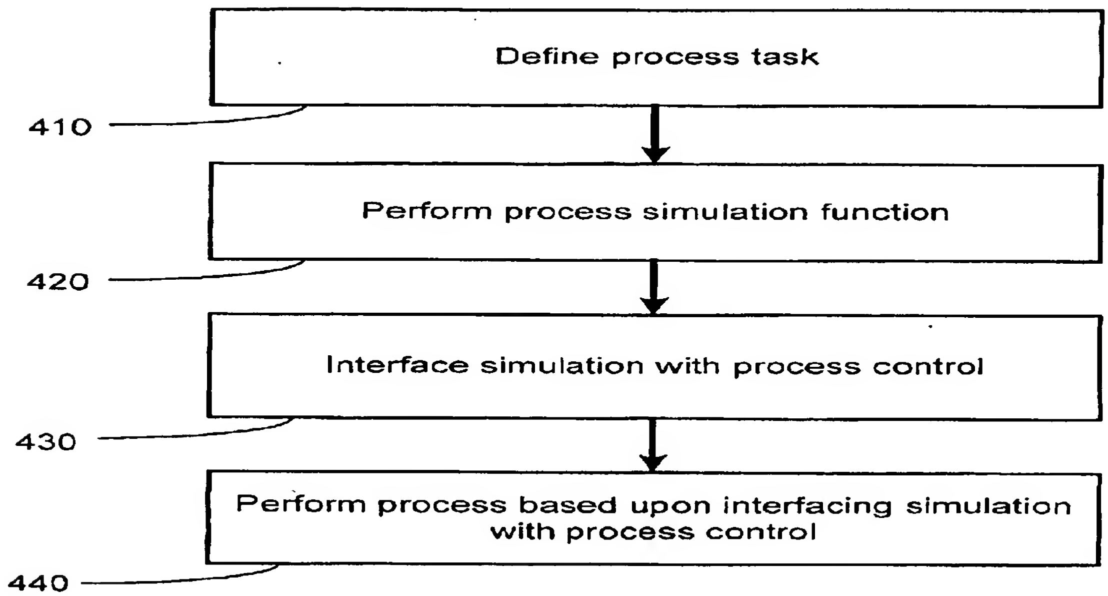

FIGURE 4

With reference to Figure 4, Sonderman et al disclose at Col. 6, lines 24-47:

> Turning now to FIG. 4, a flow chart representation of the methods in accordance with the present invention is illustrated. In one embodiment, ***the system 100 defines a process task that is to be performed (block 410).*** The process task maybe a photolithography process, an etching process, and the like. ***The system 100 then performs a process simulation function*** (block 420). A more detailed description of the process simulation function described in block 420, is illustrated below. In one embodiment, a simulation data set results from the execution of the process simulation function.
>
> ***Once the system 100 performs the process simulation function, the system 100 performs an interfacing function***, which facilitates interfacing of the simulation data with the process control environment 180 (block 430).

> The process control environment 180 can utilize the simulation data in order to modify or define manufacturing control parameters that control the actual processing steps performed by the system 100. ***Once the system 100 interfaces the simulation data with the process control environment 180, the system 100 then performs a manufacturing process*** based upon the manufacturing parameters defined by the process control environment 180 (block 440). [Emphasis added]

Hence, the process flow in Sonderman et al is straightforward:

1) define process to be modeled,
2) model process for simulation result,
3) interface simulation result to processor, and then
4) run the process under control based on the pre-existing simulation result.

Note also that this sequence in Sonderman et al means that Sonderman et al do not disclose inputting process data relating to an actual process being performed by the semiconductor processing tool, as also claimed. Rather, Sonderman et al ould have to use data from previous runs to produce a simulation result.

Accordingly, Applicant respectfully submits that Sonderman et al. do not disclose and indeed ***teach away*** from the present invention.

Furthermore, the deficiencies in Sonderman et al are not overcome by Kee et al. In the present case, the Office Action in rejecting the present claims supplements the teachings of Sonderman et al with the teachings of Kee et al.

M.P.E.P. § 2143.01(II) states that

> The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art, and all teachings in the prior art must be considered to the extent that they are in analogous arts. When the teachings of two or more prior art references conflict, the Examiner ***must weigh the power of each reference to suggest solutions*** to one of ordinary skill in the art, considering the degree to which one reference ***might accurately discredit another***. [Emphasis added.]

It appears that, the Examiner has not considered the degree to which Kee et al discredits any suggestion that the examiner may have read into the disclosure of Sonderman et al.

For instance, Kee et al in detail disclose that:

> The modeling apparatus 101 of the instant invention may also be used to perform an inverse analysis to establish the boundary conditions or parameter values required to achieve a certain function of the thermal system. This allows the apparatus to be used to establish the appropriate process parameters and boundary conditions for the thermal system modeled. In accordance with the instant invention, the inverse analysis can be directly carried out by the modeling apparatus ***rather than using the conventional approach, which merely solves the direct problem repeatedly, in a lengthy and costly iterative process***, to determine appropriate input parameters to achieve a desired result. In other words, in accordance with the instant invention, ***once a particular thermal process is modeled for a particular set of control parameters***, the device may then be used to automatically obtain the necessary control parameters to achieve a desired result by providing the modeling apparatus with parameters corresponding to the desired result.
>
> To carry out the inverse analysis, the modeling apparatus 101 includes an inverse parameter input section 104 also connected to input device 103. A user inputs into the modeling apparatus 101 parameters corresponding to desired results, e.g., desired temperature characteristics of the system, which are stored in memory 108. The processing unit 110, under control of modeling program 111, ***uses the previously generated model*** of the thermal system and the parameters held in memory 108 and derives or predicts particular control parameters to meet the constraints entered through the inverse parameter input section 104. This process is more fully described below in connection with the examples provided.[2] [emphasis added]

Hence, Kee et al explicitly disclose that the ***predicted*** model of the thermal system is used to design and control the thermal system. Kee et al exemplify the difficulties of a conventional approach which merely solves the spectral radiation transport equations through "a lengthy and costly process." These problems forced Kee et al to use ***pre-generated model results*** for a control process.

The Supreme Court in *KSR International Co. v. Teleflex Inc. et al. 2007 U.S. LEXIS 4745* reinforced the role of *Graham* factors and "teaching away" in deciding obviousness. The Court stated that:

> In *United States v. Adams*, 383 U. S. 39, 40 (1966), a companion case to *Graham*, the Court considered the obviousness of a wet battery that varied

[2] Kee et al, col. 4, lines 21-50.

> from prior designs in two ways: It contained water, rather than the acids conventionally employed in storage batteries; and its electrodes were magnesium and cuprous chloride, rather than zinc and silver chloride. The Court recognized that when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result. 383 U. S., at 50-51. It nevertheless rejected the Government's claim that Adams's battery was obvious. The Court relied upon the corollary principle that when the prior art ***teaches away*** from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious. *Id.*, at 51-52. When Adams designed his battery, the prior art warned that risks were involved in using the types of electrodes he employed. The fact that the elements worked together in ***an unexpected and fruitful manner*** supported the conclusion that Adams's design was ***not obvious*** to those skilled in the art. [Emphasis added.]

In the present situation, the claimed method of performing a first principles simulation ***for the actual process being performed during performance of the actual process*** produces ***more than an expected result*** in that Sonderman et al (in having to develop a ***new control inputs*** for each subsequent wafer) can not compensate for real time excursions from the existing model occurring while the wafer being processed. In other words, the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process using input data from the actual process that is being run. Hence, the claimed processes and systems produce ***an unexpected result***.

Viewed differently, Applicants' position on this matter is consistent with a number of the *Graham* factors identified in M.P.E.P. § 2141 III as objective evidence of non-obviousness.

The failure of both Sonderman et al and Kee et al to produce themselves the claimed invention due to the real and technical problems encountered represents ***a failure of others*** to produce the claimed invention. Moreover, the achieving of a system which can perform a first principles simulation for the actual process being performed during performance of the actual process provides ***an unexpected result***, as compared to the prior art capability.

For all these reasons, Applicant submits that the present invention patentably defines over Sonderman et al and Kee et al.

Regarding the provisional double-patenting rejection:

Applicant submits that a terminal disclaimer can be filed, if the claims in the present application and the claims in the co-pending Application Nos. 10/673,138; 10/673,467; 10/673,501; 10/673,507; 10/673,583; and 10/673,583 remain obvious in view of each other at the time of allowance of either of these applications. Indeed, M.P.E.P. § 804.02 IV states that, prior to issuance, it is necessary to disclaim each one of the double patenting references applied. Hence, Applicant respectfully requests that the examiner contact the undersigned should the present arguments be accepted and should the case be otherwise in a condition for allowance. At that time, a terminal disclaimer can be supplied to expedite issuance of this case.

Conclusion:

As discussed above, the issues identified in the outstanding Office Action for this patent application have been addressed, placing all the claims in a condition for allowance.

Consequently, in view of the above discussions, the application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Customer Number
22850

Steven P. Weihrouch
Registration No. 32,829
Attorney of Record
Ronald A. Rudder, Ph.D.
Registration No. 45,618

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)
EDG:RAR:clh

I:\ATTY\RAR\AMENDMENTS\231753US\RESPONSE-TO-OA01222007-2.DOC